In the Claims:

1. (Currently Amended) A system that executes code while processing data operations using a non-volatile memory device, comprising:

~~CPU/Bus/Controller~~ host for ~~controlling~~ accessing said memory device;

non volatile array for holding code and data of said system;

non volatile device circuitry for controlling content and activity of said non volatile array; and

logic circuit, separate from said host, for enabling automatic suspending and/or automatic resuming of operations in response to a read request from said host.

2. (Canceled)

3. (Original) The system of claim 1, wherein said non-volatile memory device is a flash memory device.

4. (Original) The system of claim 1, wherein said logic circuit enables code execution and data storage/processing facilities within a single chip device with a single silicon die.

5. (Original) The system of claim 1, wherein said logic circuit enables code execution and data storage/processing facilities within a bank of single memory chips with single silicon dies.

6. (Currently Amended) The system of claim 1, wherein said logic circuit is embedded into the memory ~~chip~~ device.

7-9. (Canceled)

10. (Currently Amended) The system of claim 1, wherein said logic circuit is operative to monitor status of current operations in said memory ~~chip~~ device.

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11-12. (Canceled)

13. (Currently Amended) A method for executing code while processing data on a non-volatile memory device, comprising the steps of:

i. adding at least one logic circuit to operate with the non-volatile memory device[[.]];

ii. monitoring status of current operations in said memory ~~chip~~ device, by said at least one logic circuit[[.]];

iii. signaling ~~to the CPU/Bus~~ if the ~~chip~~ device is available for code execution, by said at least one logic circuit[[.]]; and

iv. ~~monitoring CPU/Bus activity~~

~~v.~~ commanding ~~chip~~ the device to suspend and/or resume ~~chip~~ device operations in response to a read request, by said at least one logic circuit.

14. (Currently Amended) A method for executing code while processing data on a non-volatile memory device, comprising the following steps:

i. adding at least one logic circuit to work with the **[[a]]** non-volatile memory ~~chip~~ device**[[.]]**;

ii. sensing a read request**[[s]]** while ~~chip~~ the device is in program/erase mode/operation, by said at least one logic circuit**[[.]]**;

iii. ~~automatic~~ in response to said sensing, entering of program and/or erase operations into suspended mode, by said at least one logic circuit**[[.]]**;

iv. signaling to CPU/Bus to ~~wait before executing further read/fetch commands~~ delay executing said read request, by said at least one logic circuit**[[.]]**;

v. turning off signal to allow CPU/Bus to ~~(automatically) continue with read/fetch commands~~ execute said read request, by said at least one logic circuit; and

vi. ~~entering~~ exiting of said ~~chip~~ device ~~into resume operations~~ from said suspended mode to continue program/erase operation, by said at least one logic circuit.

15. (Canceled)

16. (Original) A single flash memory device comprising:

a suspend logic circuit for enabling hardware initiated suspending of data processing operations; and

a resume logic circuit for enabling hardware initiated resuming of data processing operations.

17. (New) A memory device comprising:

(a) a non-volatile memory;

(b) circuitry for reading, programming and erasing said non-volatile memory; and

(c) a hardware mechanism for suspending an activity of said circuitry in response to at least one read request.

18. (New) The memory device of claim 17, wherein said hardware mechanism also is operative to resume said activity of said circuitry after said circuitry has finished processing said at least one read request.

19. (New) The memory device of claim 17, wherein said activity is erasing said non-volatile memory.

20. (New) The memory device of claim 17, wherein said activity is programming said non-volatile memory.

21. (New) The memory device of claim 17, wherein said hardware mechanism includes at least one logic circuit.

22. (New) The memory device of claim 17, wherein said suspending of said activity includes:

(A) indicating to a host that issued said at least one read request that execution of said at least one read request should be delayed; and

(B) subsequently, indicating to said host that the memory device is available for reading.

23. (New) The memory device of claim 17, wherein said hardware mechanism is further operative to:

(iii) monitor said processing of said at least one read request to determine when said circuitry has finished processing said at least one read request.

24. (New) A method for managing a memory device that includes a non-volatile memory and that is accessed by a host, comprising the steps of:

(a) commencing an operation selected from the group consisting of erasing the non-volatile memory and programming the non-volatile memory, by the memory device;

(b) during said operation, requesting a read operation, by the host; and

(c) in response to said request, suspending said operation, by the memory device.

25. (New) The method of claim 24, further comprising the step of:

(d) in response to said request, signaling to the host to delay execution of said request, by the memory device.

26. (New) The method of claim 25, further comprising the step of:

(e) in response to said signal, delaying execution of said request, by the host.

27. (New) The method of claim 26, further comprising the step of:

(f) signaling the host to resume execution of said request, by the memory device.

28. (New) The method of claim 27, further comprising the steps of:

(g) subsequent to said suspending, monitoring a conclusion of read requests from the host, by the memory device; and

(h) upon detecting said conclusion, resuming said operation, by the memory device.